and supplying said offset cancel voltage to said A/D converter.

26.   (ONCE AMENDED) A signal processor for receiving data information as an analog signal and processing said analog signal, comprising:

an A/D converter converting said analog signal to a digital signal;

an offset cancel circuit, connected to said A/D converter, supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit including,

a comparator receiving said digital signal, and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result;

an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result ; and

an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

27.   (ONCE AMENDED) A signal processor for processing a data information signal and a servo information signal, both read from a recording medium, said signal processor comprising:

a servo information processing circuit processing servo information; and

a data information processing circuit, connected to said servo information processing circuit, receiving data information as an analog signal and processing said analog signal, said data information processing circuit includes,

A) an A/D converter receiving said analog signal from an input terminal and converting said analog signal to a digital signal, to output said digital signal from an output terminal;

B) a switch connected to said input terminal of said A/D converter; and

C) an offset cancel circuit, connected between said input terminal and an output terminal of said A/D converter, supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

C1)   a control circuit, connected to said switch, setting said switch off to inhibit supply of said analog signal to said A/D converter when said servo information processing circuit is performing a servo information process,

2

C2)   a comparator connected to said comparator, receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result,

C3)   an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result, and

C4)   an offset voltage generator connected to said arithmetic operation unit, generating an offset cancel voltage for canceling said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

28.   (ONCE AMENDED) The signal processor according to claim 27, further comprising:

D)   an amplifier, connected to said input terminal of said A/D converter and said control circuit, amplifying said analog signal and said offset cancel voltage by a first amplification factor, wherein said amplifier amplifies said offset cancel voltage by a second amplification factor which is higher than said first amplification factor,

wherein said arithmetic operation unit has a reduced offset change amount inversely proportional to an increase ratio of said first amplification factor to said second amplification factor, and wherein said control circuit is connected to said comparator and said arithmetic operation unit, and

wherein when said digital value lies within said predetermined offset value range, said control circuit controls said amplifier in such a way as to amplify said offset cancel voltage by said second amplification factor and controls said arithmetic operation unit to perform addition based on said reduced offset change amount.

29.   (ONCE AMENDED) A circuit suitable for canceling an offset voltage of an A/D converter, said A/D converter samples an analog data signal including an analog sinusoidal signal in order to convert said analog data signal to a digital signal, said circuit comprising:

a sampling control circuit controlling said A/D converter so that an interval between first and third sampling points and an interval between second and fourth sampling points for said analog sinusoidal signal each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order;

an arithmetic operation unit receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter; and

an offset voltage generator receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and supplying said offset cancel voltage to said A/D converter.

30.   (ONCE AMENDED) A signal processor for receiving an analog data signal including an analog sinusoidal signal recorded on a recording medium, and processing said analog data signal, said signal processor comprising:

an A/D converter converting said analog sinusoidal signal and said analog data signal to digital signals; and

an offset cancel circuit, connected to said A/D converter, supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

a sampling control circuit controlling said A/D converter so that an interval between first and third sampling points and an interval between second and fourth sampling points for said analog sinusoidal signal each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order;

an arithmetic operation unit receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter; and

an offset voltage generator receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and supplying said offset cancel voltage to said A/D converter.

31.   (ONCE AMENDED) A signal processor for processing a data information signal and a servo information signal, both read from a recording medium, said signal processor comprising:

a servo information processing circuit processing servo information,

a data information processing circuit receiving data information as an analog data signal including an analog sinusoidal signal and processing said analog data signal, said data

4

information processing circuit including,

A)   an A/D converter receiving said analog data signal from an input terminal and converting said analog data signal to a digital signal to output said digital signal from an output terminal;

B)   a switch connected to said input terminal of said A/D converter; and

C)   an offset cancel circuit, connected between said input terminal and output terminal of said A/D converter, supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

C1)   a sampling control circuit controlling said A/D converter so that an interval between first and third sampling points and an interval between second and fourth sampling points for said analog sinusoidal signal each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first through fourth digital values are output from said A/D converter in a sampling order,

C2)   an arithmetic operation unit receiving one of a set of said first and third digital values and a set of said second and fourth digital values, and computing an average value thereof to output said obtained average value as an offset voltage value for said A/D converter, and

C3)   an offset voltage generator receiving said offset voltage value, for generating an offset cancel voltage to cancel said offset voltage, and supplying said offset cancel voltage to said A/D converter.

---

34.   (ONCE AMENDED) A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, said method comprising:

determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to determine an offset change amount;

accumulating said offset change amount;

stopping said accumulating, to determine an accumulated offset change amount, when said digital value lies within said predetermined offset allowance value; and

generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount.

35.   (ONCE AMENDED) A method of canceling an offset voltage of an A/D converter for sampling an analog data signal including an analog sinusoidal signal to convert said analog

data signal to a digital signal, said method comprising:

controlling said A/D converter so that an interval between first and third sampling points and an interval between second and fourth sampling points for said analog sinusoidal signal each is 180 degrees when said analog sinusoidal signal is supplied to said A/D converter, whereby digital signals having first to fourth digital values are output from said A/D converter in a sampling order;

computing an average value of one of a set of said first and third digital values and a set of said second and fourth digital values, said obtained average value being an offset voltage value for said A/D converter; and

generating an offset cancel voltage to cancel said offset voltage in accordance with said offset voltage value.

Please ADD the following NEW claims:

51.   (NEW) The circuit according to claim 25, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

52.   (NEW) The circuit according to claim 25, wherein the arithmetic operation unit calculates the offset change amount on the basis of the comparison result and an offset unit change.

53.   (NEW) The circuit according to claim 25, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

54.   (NEW) The circuit according to claim 25, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

55.   (NEW) The signal processor according to claim 26, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

56.   (NEW) The signal processor according to claim 26, wherein the arithmetic

operation unit calculates the offset change amount on the basis of the comparison result and an offset unit change.

57. (NEW) The signal processor according to claim 26, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

58. (NEW) The signal processor according to claim 26, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

59. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

60. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit calculates the offset change amount on the basis of the comparison result and an offset unit change.

61. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

62. (NEW) The signal processor according to claim 27, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

63. (NEW) A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, said method comprising:

determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to determine an offset change amount;

accumulating said offset change amount; and

generating an offset cancel voltage for canceling said offset voltage in accordance with

said accumulated offset change amount.

64.   (NEW) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator receiving said digital signal and for comparing a digital value of said digital signal with a predetermined offset value;

an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result, wherein said addition result is initialized to a predetermined initial value; and

an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

65.   (NEW) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator to receive said digital signal and compare a digital value of said digital signal with a predetermined offset value;

an arithmetic operation unit, connected to said comparator, to calculate a value of the changed amount of offset between the digital value and predetermined offset value, and output a result; and

an offset voltage generator, connected to said arithmetic operation unit, to generate an offset cancel voltage to cancel said offset voltage in accordance with the result, and supply said offset cancel voltage to said A/D converter.

8